What is claimed is:

1. A semiconductor device, comprising:

a support substrate;

an insulating layer formed on the support substrate;

a first semiconductor layer formed on the insulating layer;

a first high breakdown voltage transistor formed in the first semiconductor layer;

a second semiconductor layer formed on the insulating layer;

a second high breakdown voltage transistor formed in the second semiconductor layer;

a first isolation region formed between the first semiconductor layer and the second semiconductor layer, the first isolation region having a depth that reaches the insulating layer;

a third semiconductor layer formed on the insulating layer;

a first low breakdown voltage transistor formed in the third semiconductor layer;

a second low breakdown voltage transistor formed in the third semiconductor layer; and

a second isolation region formed in the third semiconductor layer between the first low breakdown voltage transistor and the second first low breakdown voltage transistor, the second isolation region having a depth that does not reach the insulating layer.

2. A semiconductor device according to Claim 1, further comprising:

a third isolation region formed between the second semiconductor layer and the third semiconductor layer, the third isolation region having a depth that reaches the insulating layer.

3. A semiconductor device according to Claim 1,

wherein the first semiconductor layer, the second semiconductor layer, and the third semiconductor layer are all of equal thickness.

4. A semiconductor device according to Claim 2,

wherein the first semiconductor layer, the second semiconductor layer, and the third semiconductor layer are all of equal thickness.

5. A semiconductor device according to Claim 3,

wherein the first semiconductor layer, the second semiconductor layer, and the third semiconductor layer are respectively 500 to 2,000nm thick.

6. A semiconductor device according to Claim 4,

wherein the first semiconductor layer, the second semiconductor layer, and the third semiconductor layer are respectively 500 to 2,000nm thick.

7. A semiconductor device according to Claim 1,

wherein surfaces of the first semiconductor layer, the second semiconductor layer, and the third semiconductor layer are at a same level.

8. A semiconductor device according to Claim 2,

wherein surfaces of the first semiconductor layer, the second semiconductor layer, and the third semiconductor layer are at a same level.

9. A semiconductor device according to Claim 1,

wherein the first and second high breakdown voltage transistors further comprise:

a first gate insulating layer formed above a channel region; and

a second gate insulating layer formed above an offset region,

wherein the second gate insulating layer is thicker than the first gate insulating layer.

10. A semiconductor device according to Claim 2,

wherein the first and second high breakdown voltage transistors further comprise:

a first gate insulating layer formed above a channel region; and

a second gate insulating layer formed above an offset region,

wherein the second gate insulating layer is thicker than the first gate insulating layer.

11. A method of manufacturing a semiconductor device, the method comprising the steps of:

preparing a substrate including a support substrate, an insulating layer, and a

semiconductor layer;

forming a first isolation region and a third isolation region with a depth that reaches the insulating layer such that the semiconductor layer is divided a first semiconductor layer, a second semiconductor layer, and a third semiconductor layer;

forming a second isolation region in the third semiconductor layer with a depth that does not reach the insulating layer;

forming a first high breakdown voltage transistor in the first semiconductor layer;

forming a second high breakdown voltage transistor in the second semiconductor layer;

forming a first low breakdown voltage transistor in the third semiconductor layer; and

forming a second low breakdown voltage transistor in the third semiconductor layer that is adjacent to the first low breakdown voltage transistor with the second isolation region therebetween.

12. A method of manufacturing a semiconductor device according to Claim 11,

wherein the steps of forming the first and second high breakdown voltage transistors, further comprising the steps of:

forming an offset insulating layer above an offset region; and

forming a first gate insulating layer above at least a channel region and the offset region, thereby forming a second gate insulating layer above the offset region, the second gate insulating layer including the offset insulating layer and the first gate insulating layer.

13. A method of manufacturing a semiconductor device according to Claim 12,

wherein the steps of forming the offset insulating layer and the second isolation region are performed by the same step.

14. A method of manufacturing a semiconductor device according to Claim 11,

wherein the second isolation region is formed by trench isolation.

15. A method of manufacturing a semiconductor device according to Claim 12,

wherein the second isolation region is formed by trench isolation.

16. A method of manufacturing a semiconductor device according to Claim 11,

wherein the second isolation region is formed by LOCOS.

17. A method of manufacturing a semiconductor device according to Claim 12, wherein the second isolation region is formed by LOCOS.

18. A method of manufacturing a semiconductor device according to Claim 11, wherein the second isolation region is formed by semi-recessed LOCOS.

19. A method of manufacturing a semiconductor device according to Claim 12, wherein the second isolation region is formed by semi-recessed LOCOS.

20. A semiconductor device comprising:

a support substrate;

an insulating layer formed on the support substrate;

a high breakdown voltage transistor;

a low breakdown voltage transistor, wherein the high breakdown voltage transistor is adjacent to a first isolation region having a depth that reaches the insulating layer, and the low breakdown voltage transistor is adjacent to a second isolation region having a depth that does not reach the insulating layer.

21. A method of manufacturing a semiconductor device, the method comprising the steps of:

preparing a substrate including a support substrate and an insulating layer;

forming a first isolation region having a depth that reaches the insulating layer;

forming a second isolation region having a depth that does not reach the insulating layer;

forming a first high breakdown voltage transistor in a region adjacent to the first isolation region; and

forming a first low breakdown voltage transistor in a region adjacent to the second isolation region.

22. A method of manufacturing a semiconductor device according to Claim 11, wherein the first and third isolation regions are made up of oxide films formed by thermal oxidation.

23. A method of manufacturing a semiconductor device according to Claim 11,

wherein the first and second isolation regions are formed made up of oxide films formed by etching first and second trenches.

24. A method of manufacturing a semiconductor device according to Claim 23, wherein the first and second trenches are formed simultaneously.

25. A method of manufacturing a semiconductor device according to Claim 11, wherein the first and third isolation regions are formed by etching first and second trenches, and further including the step of oxidizing base parts of the trenches to form oxide films, wherein the formation of the trenches is combined with the formation of the oxide film.